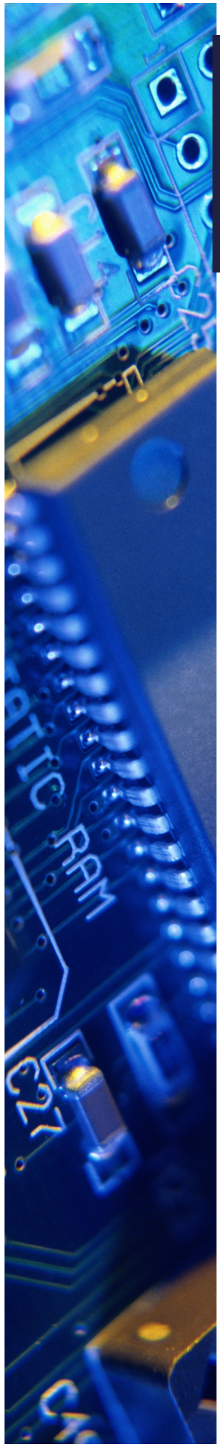

UNIVERSIDADE da MADEIRA

AWAIBA
a CMOSIS company

Multi-Camera Synchronization for the NanEye CMOS Image Sensor

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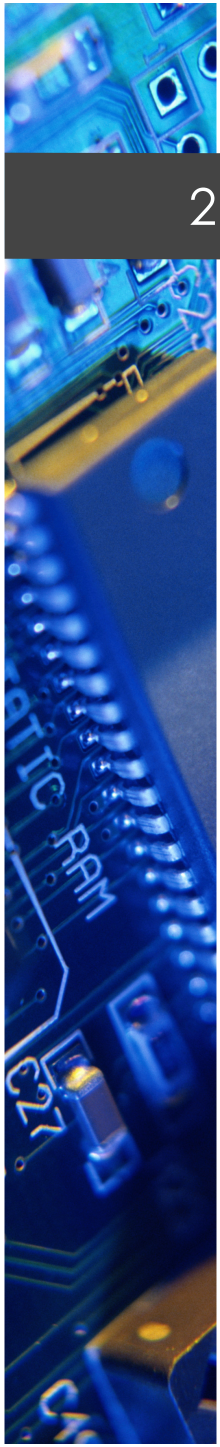
Centro de Competência de
CIÊNCIAS EXACTAS E DA ENGENHARIA

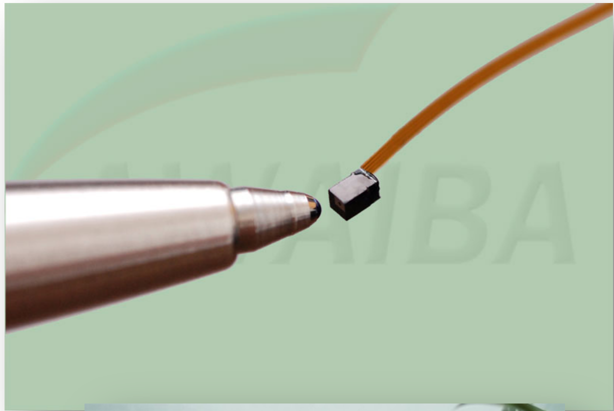


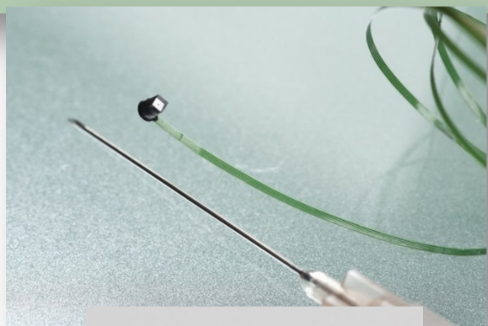
Summary

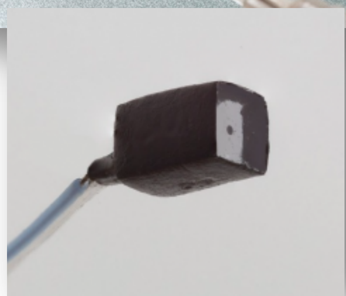
- Introduction
  - NanEye CMOS Image Sensor
  - Motivation
  - Video Synchronization
- Multi-Camera Synchronization Core
  - Problem Analysis
  - Proposed Solution
  - Results
- Advanced illumination control algorithm in VHDL
- Conclusion

Introduction

NanEye CMOS Image Sensor







- Characteristics:
  - **1,0x1,0x1,65 mm**
  - 250x250 pixels (62,5k)
  - **44 fps nominal**
  - Rolling Shutter
  - **10 bit digital output**
  - Semi duplex LVDS interface
  - **No need for external components (embedded LVDS driver and on-chip decoupling capacitors)**

Introduction

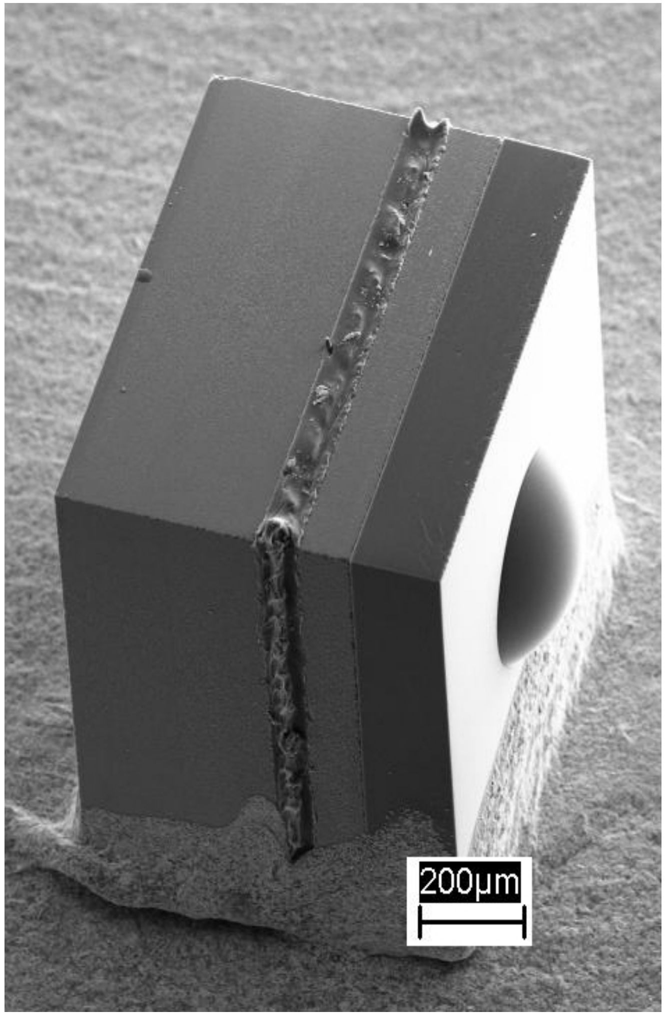
➨ **NanEye** CMOS Image Sensor

Digital image sensors use architectures suitable for scaling up to several Mega pixels resolution.

Only part of the chip is used for the pixel matrix; peripheral area is used for ADC, Low power charge pumps, exposure control, colour reconstruction and mobile processor interfaces.

Non mandatory features were removed or redesigned to achieve a chip periphery below 90 μ m on each side of the matrix.

On a chip with 700 μ m side length this leaves less than 0.2mm^2 for peripheral electronics.

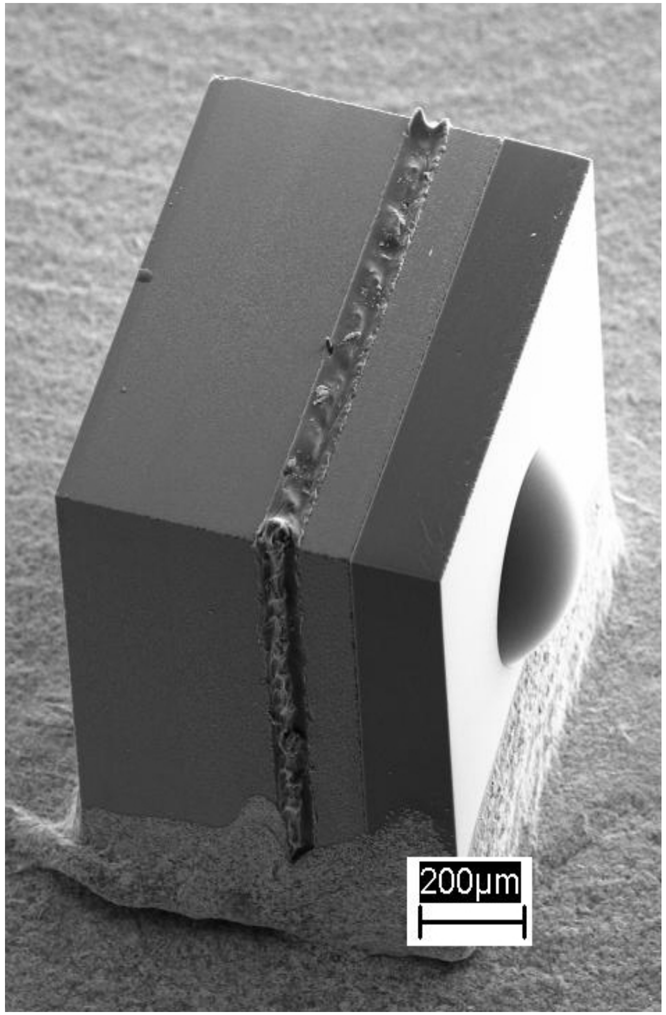


Introduction

➨ **NanEye** CMOS Image Sensor

Architecture was optimized to avoid the need of passive components such as decoupling capacitors, allowing the cameras to run up to 3m cable length and transmit digital output without coaxial shielding or loss of quality.

The size optimized sensor is not enough to build minimal size camera modules.

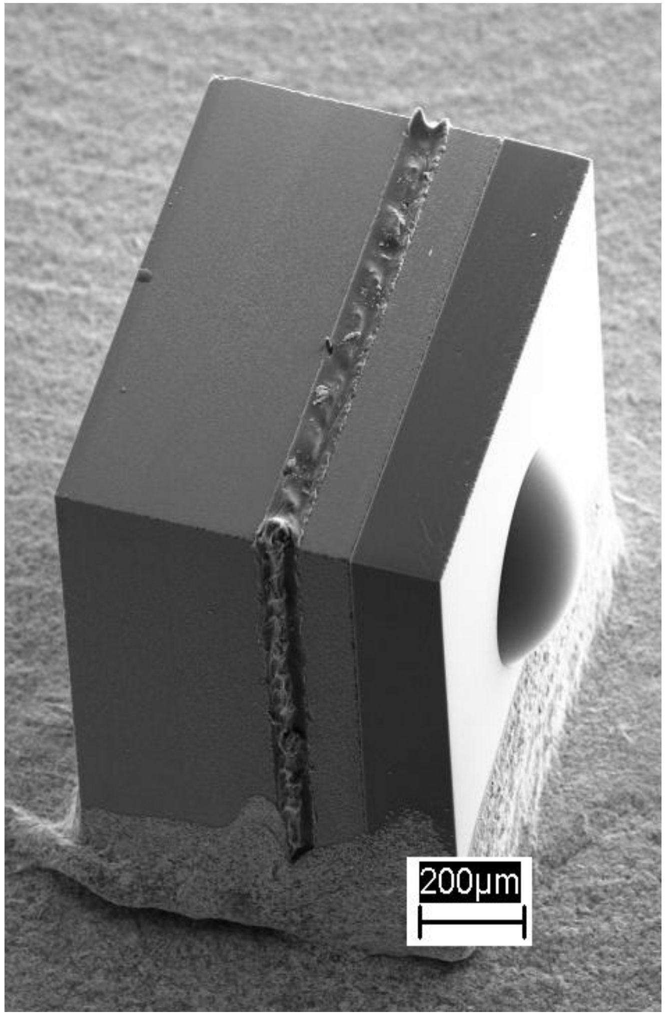


Introduction

➨ **NanEye** CMOS Image Sensor

To permit the chip packaging on such small footprint, the electrical connection to the image is made by **Chip Scale packaging technology**, providing electrical contact by "drilling" tiny via holes through the silicon and connecting from solder balls on the back side to the active electronics on the front side.

True Silicon Via permits to keep the overall device and package size to exactly the outline of the image sensor circuit and does not require extra area for bond wires or connections over the device sides.



Introduction

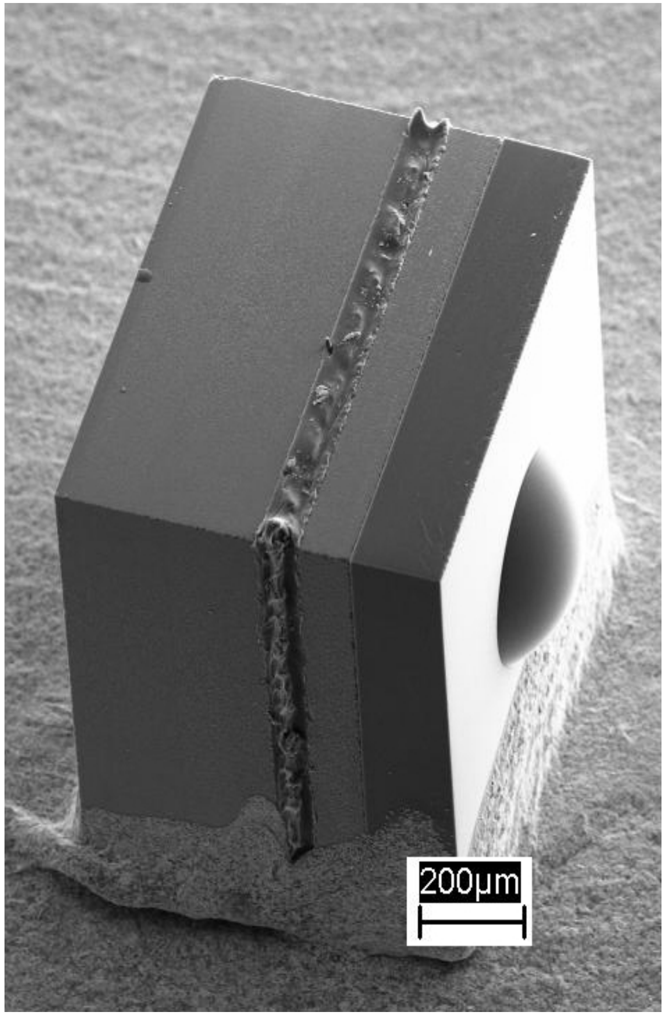
➨ **NanEye** CMOS Image Sensor

Lens at the 1mm scale is a challenge.

-**Lenses were etched out of Quartz glass wafers** and the full wafer stack was assembled on the CMOS image sensor wafer.

-Unique technology developed by AWAIBA with several research institutes.

-It also provides a great economy of scale when slicing up pizza size wafer stacks to 1mm or smaller camera modules, **several thousand cameras result from one single wafer**, allowing for low cost at high volumes.



Introduction

NanEye CMOS Image Sensor

- Applications:
  - **Medical endoscopy**
  - Dental imaging
  - **Surgical robots**
  - Single use medical equipment

Introduction

Motivation

NanEye

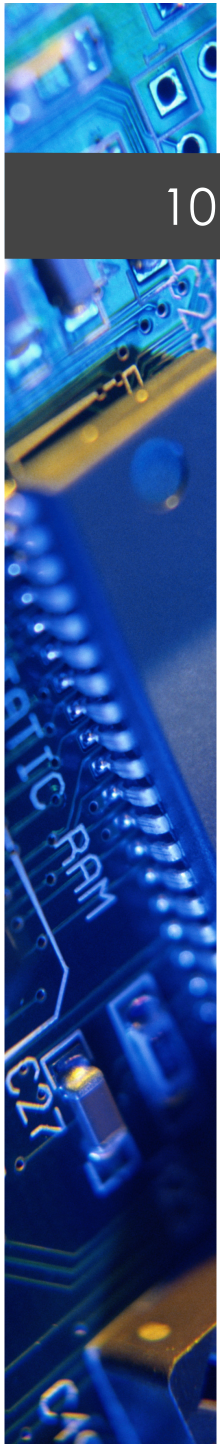
NanEye

NanEye Stereo

3D Imaging

Phase and Frequency Synchronization

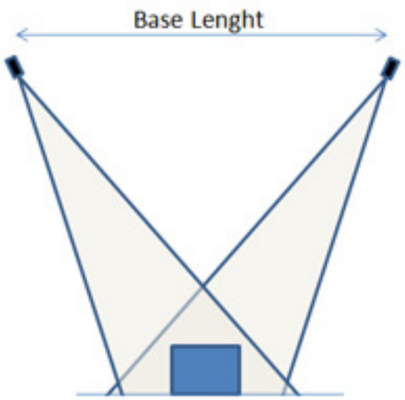
- Advantages:
  - **More precise hand-eye coordination**
  - Realistic tissue structure representation
  - **Smoother learning curve for the equipment user**
  - Precise operation, which implies more comfort for the patient
  - **Less time required to perform procedure**



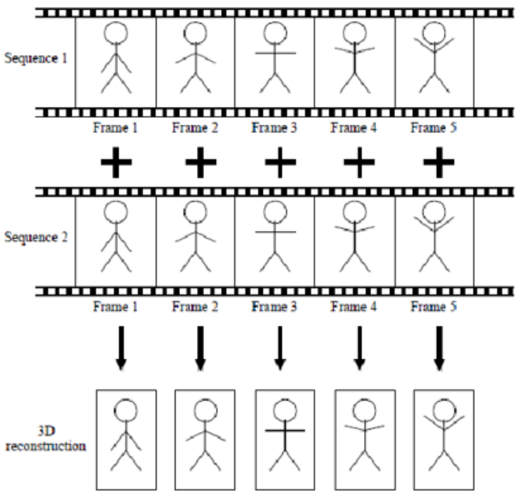
Introduction

➨ Video Synchronization

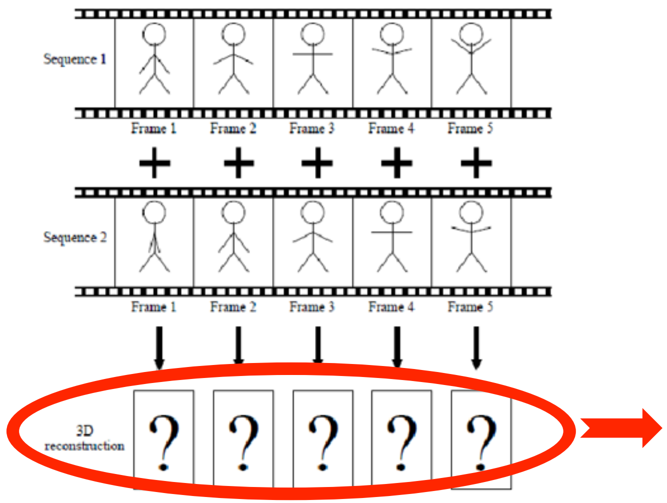
- **A processing algorithm merges the two data streams into a single set of images**
- Simultaneously the differences between the images are interpreted to determine depth



Stereoscopic 3D Vision



a) Synchronized Video Sequences

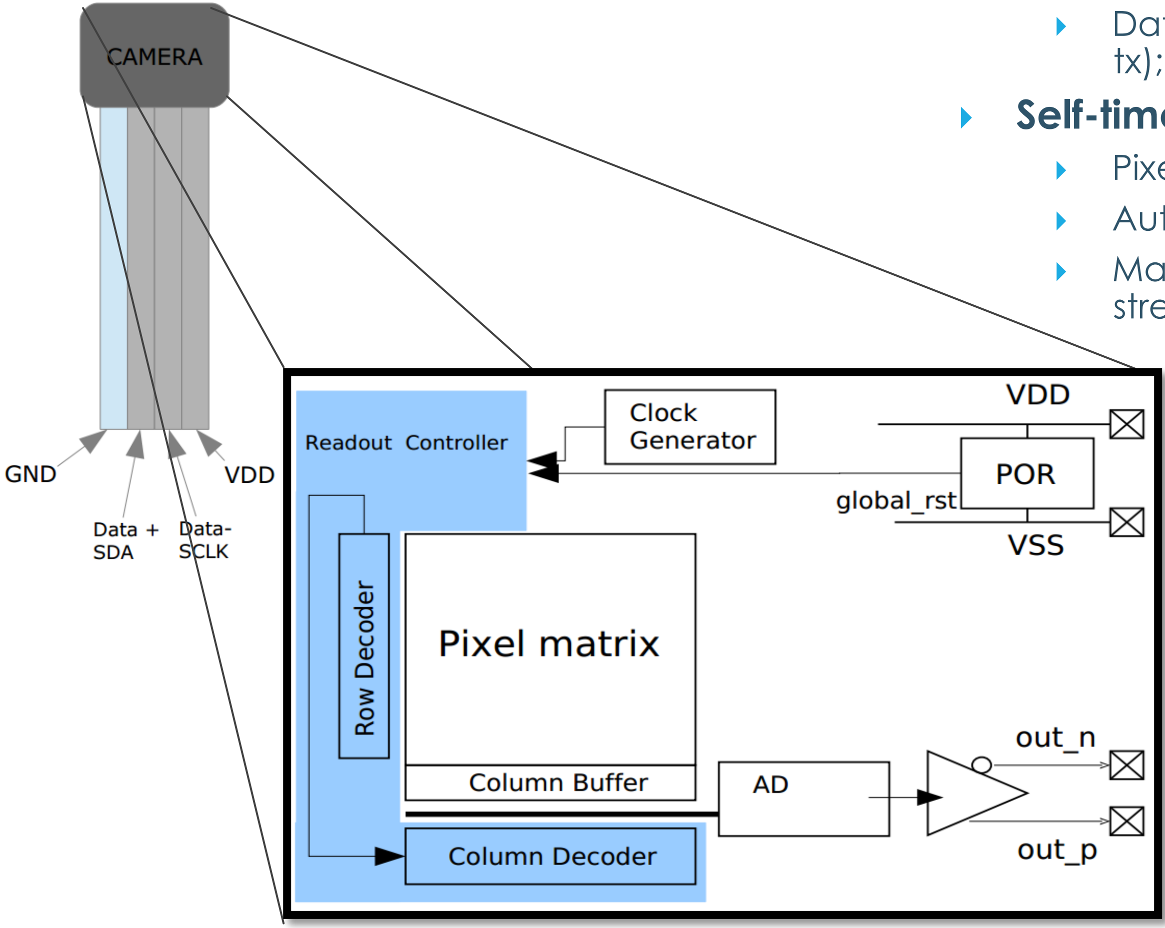


b) Non Synchronized Video Sequences

In the absence of synchronization it's not possible to combine the Frames without using an external memory and additional processing

Multi-Camera Synchronization Core

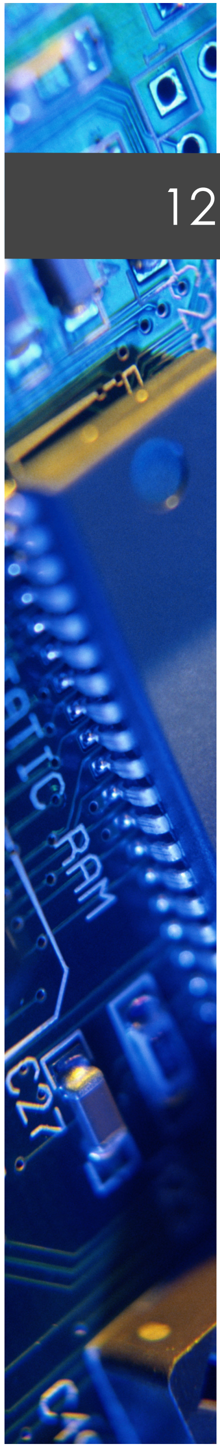
Problem Analysis



- **4 pin interface**
  - GND and VDD
  - Data+ and Data- (downstream tx); SDA and SCLK (upstream tx)
- **Self-timed Sensor**
  - Pixel clock is generated internally
  - Autonomous readout
  - Manchester encoded data stream

The pixel clock is generated by a Ring Oscillator

Multi-Camera Synchronization Core



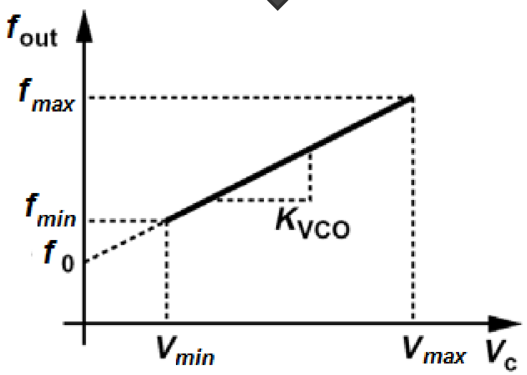
Problem Analysis

- **In the frequency domain, the NanEye sensor can then be modelled as a VCO:**

$$f_{out} = f_0 + K_{VCO} V_C$$

Oscillation frequency when Vc=0

Control Voltage



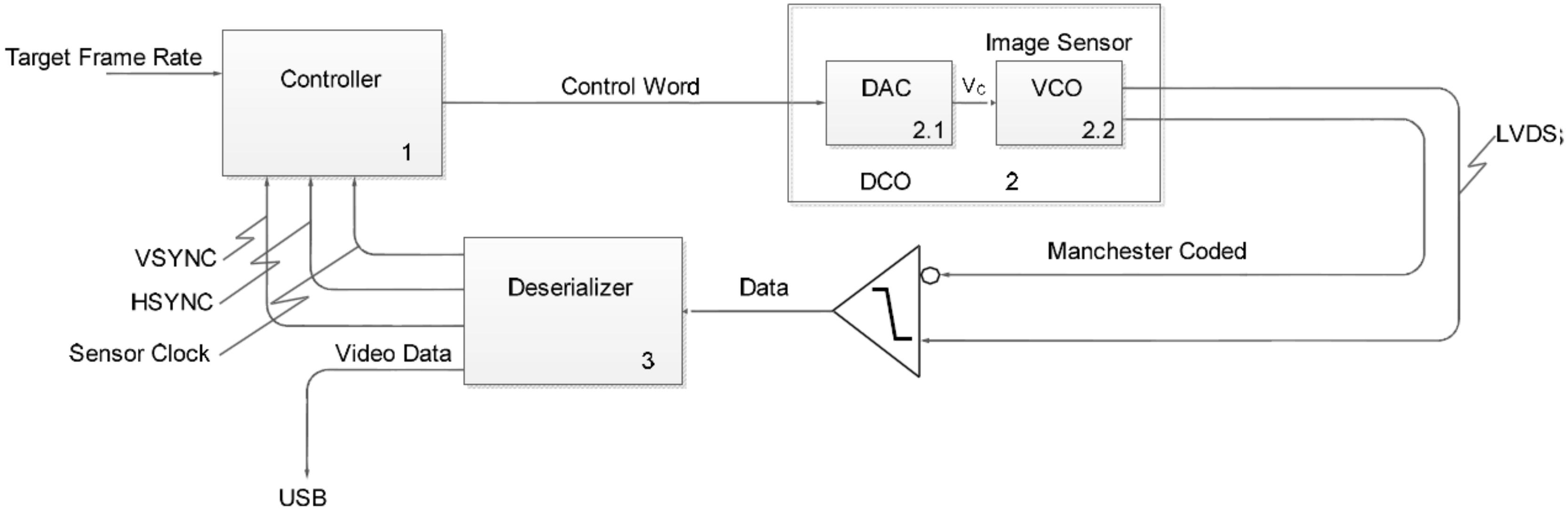
Oscillator sensibility given in Hz/V

Frequency control on the sensor is not performed through registers but through the power supply applied between VDD and GND.

Multi-Camera Synchronization Core

Problem Analysis

Control System Model



Constraints

- Time delays
- Voltage drops
- Temperature dependency
- Multiple Sensors

Multi-Camera Synchronization Core

Proposed Solution

	Frequency Control based on an ADPLL	Frequency control based on line and frame period
+	Less error Detailed Frequency control	Simplicity Ocupied area Portability Ease of Replication
−	Complexity More sensibility to pixel clock jitter Temperature dependency **<u>Not possible to generate any frequency</u>**	In principle, higher error

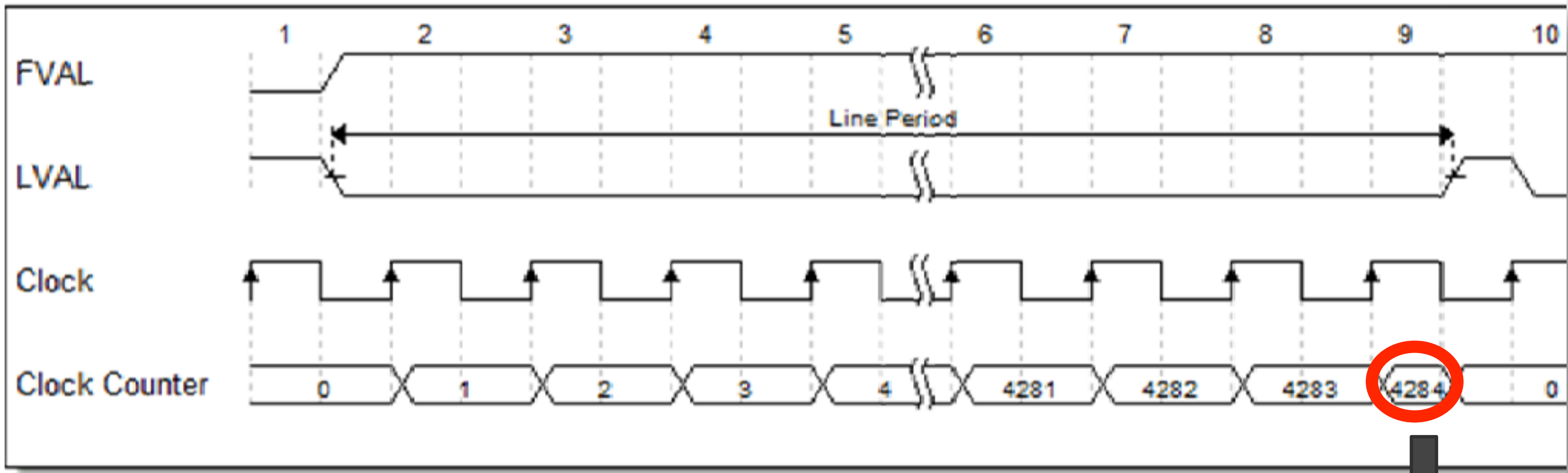
Multi-Camera Synchronization Core

Proposed Solution

- Line Period Measurement

$$T_{Line} = \frac{1/44\ fps}{253\ lines} = 89{,}83\ \mu s$$

$$Target_{Clk} = \frac{T_{Line}}{T_{System\ Clock}} = \frac{89{,}83\ \mu s}{1/48\ MHz} \cong 4312\ clocks$$

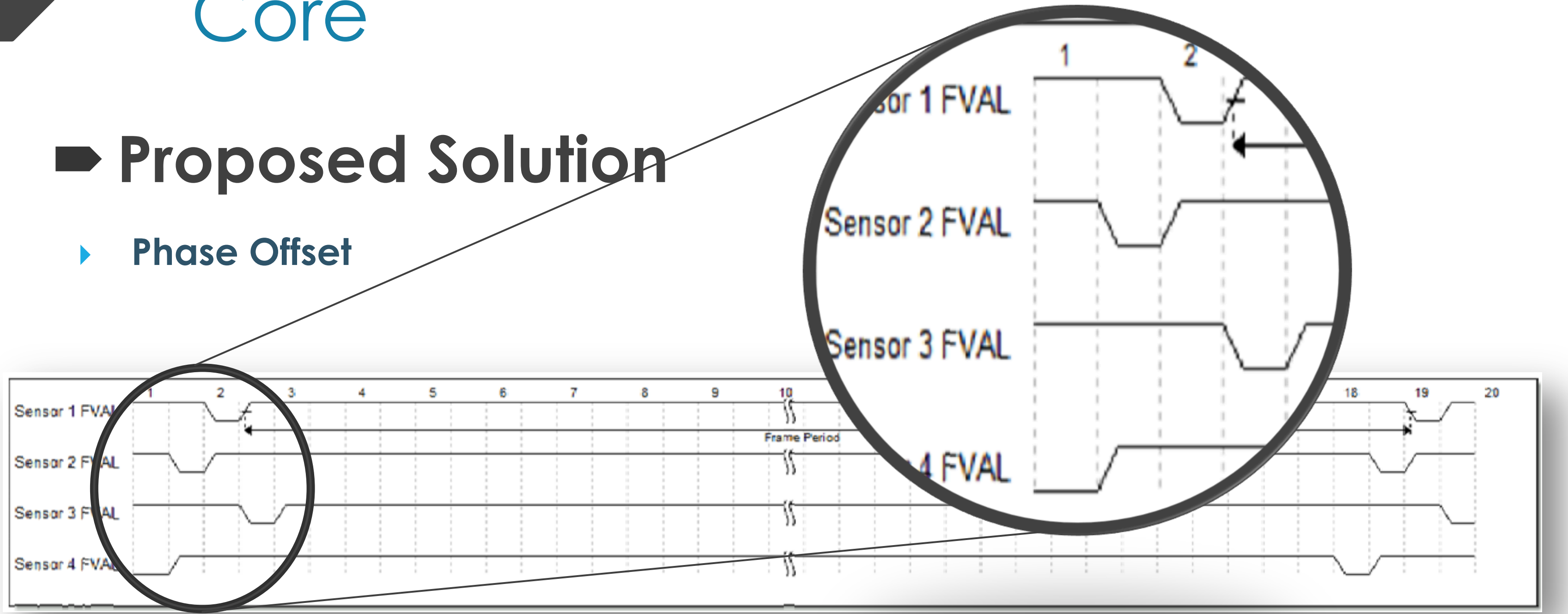


Count below Target → Frequency is too high → Vc must be lowered

Multi-Camera Synchronization Core

Proposed Solution

- **Phase Offset**



- Even if the sensors operate at the same frequency, it does not mean they are phase synchronized!

A reference is needed!!

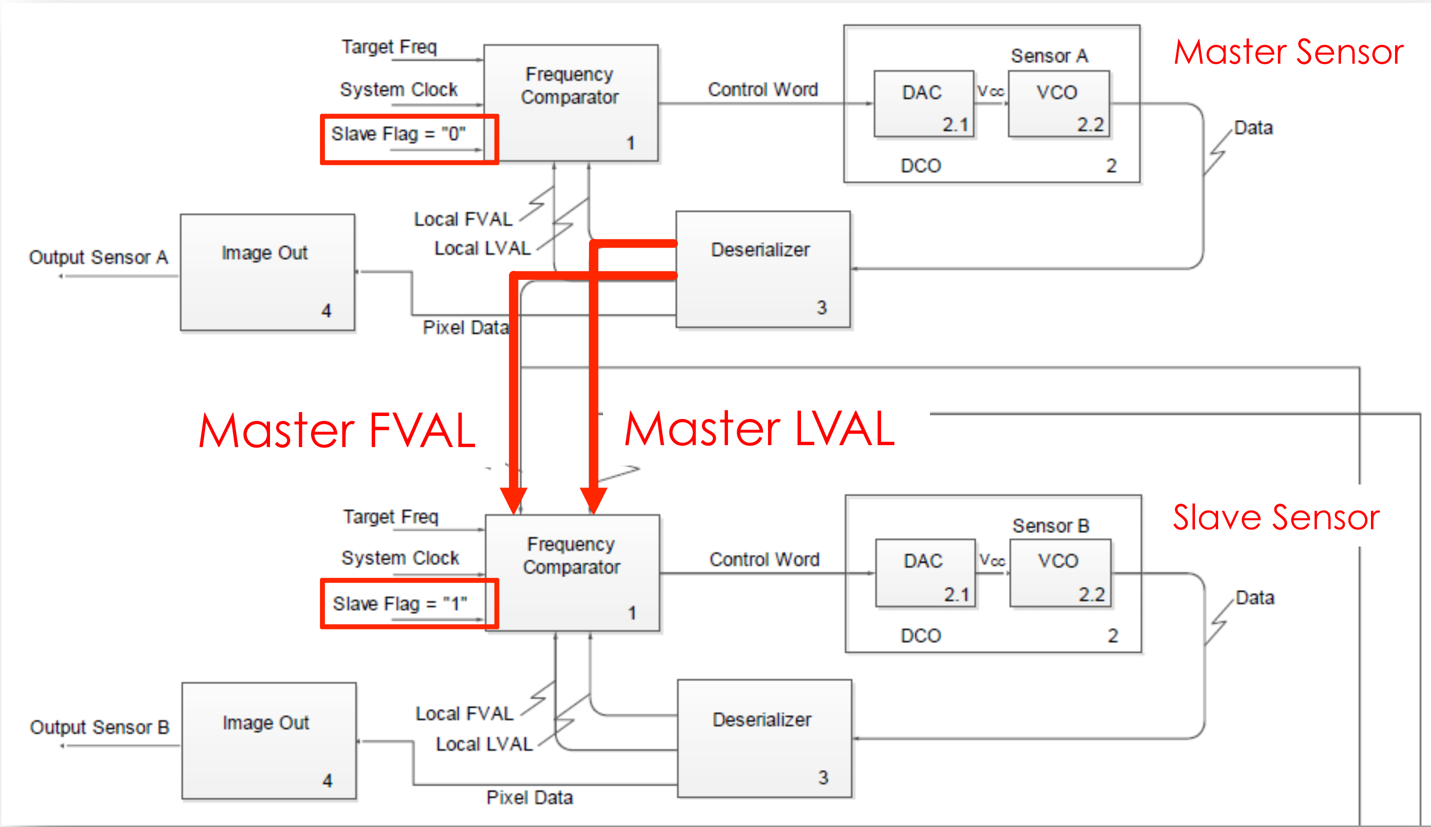
Solution:

<u>MASTER-SLAVE INTERFACE</u>

Multi-Camera Synchronization Core

Proposed Solution

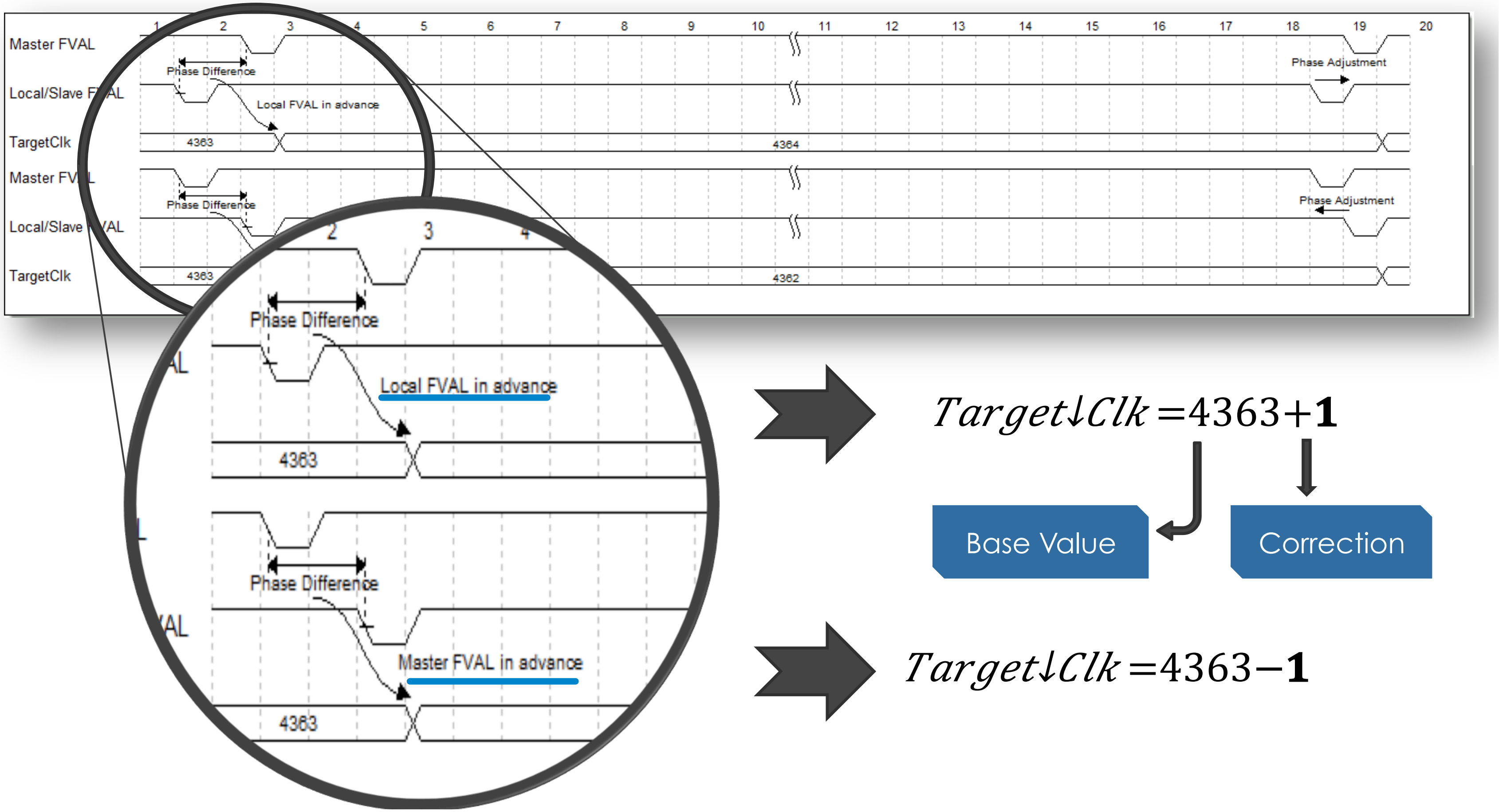
- **Master-Slave Interface**



Multi-Camera Synchronization Core

➨ Proposed Solution

- **Phase Correction**

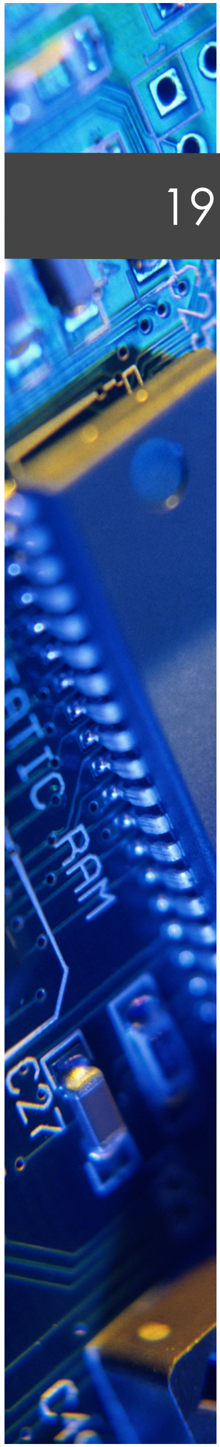


$$Target\downarrow Clk = 4363 + \mathbf{1}$$

Base Value

Correction

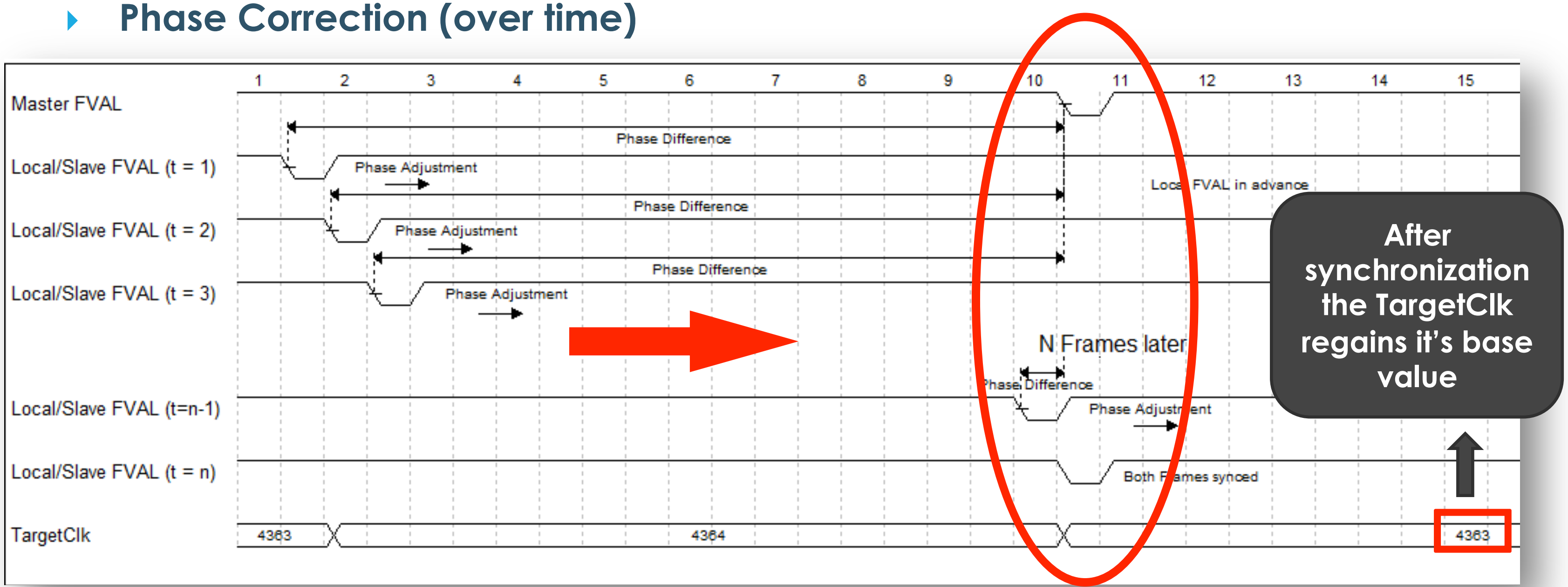
$$Target\downarrow Clk = 4363 - \mathbf{1}$$



Multi-Camera Synchronization Core

➨ Proposed Solution

- **Phase Correction (over time)**



After synchronization the TargetClk regains it's base value

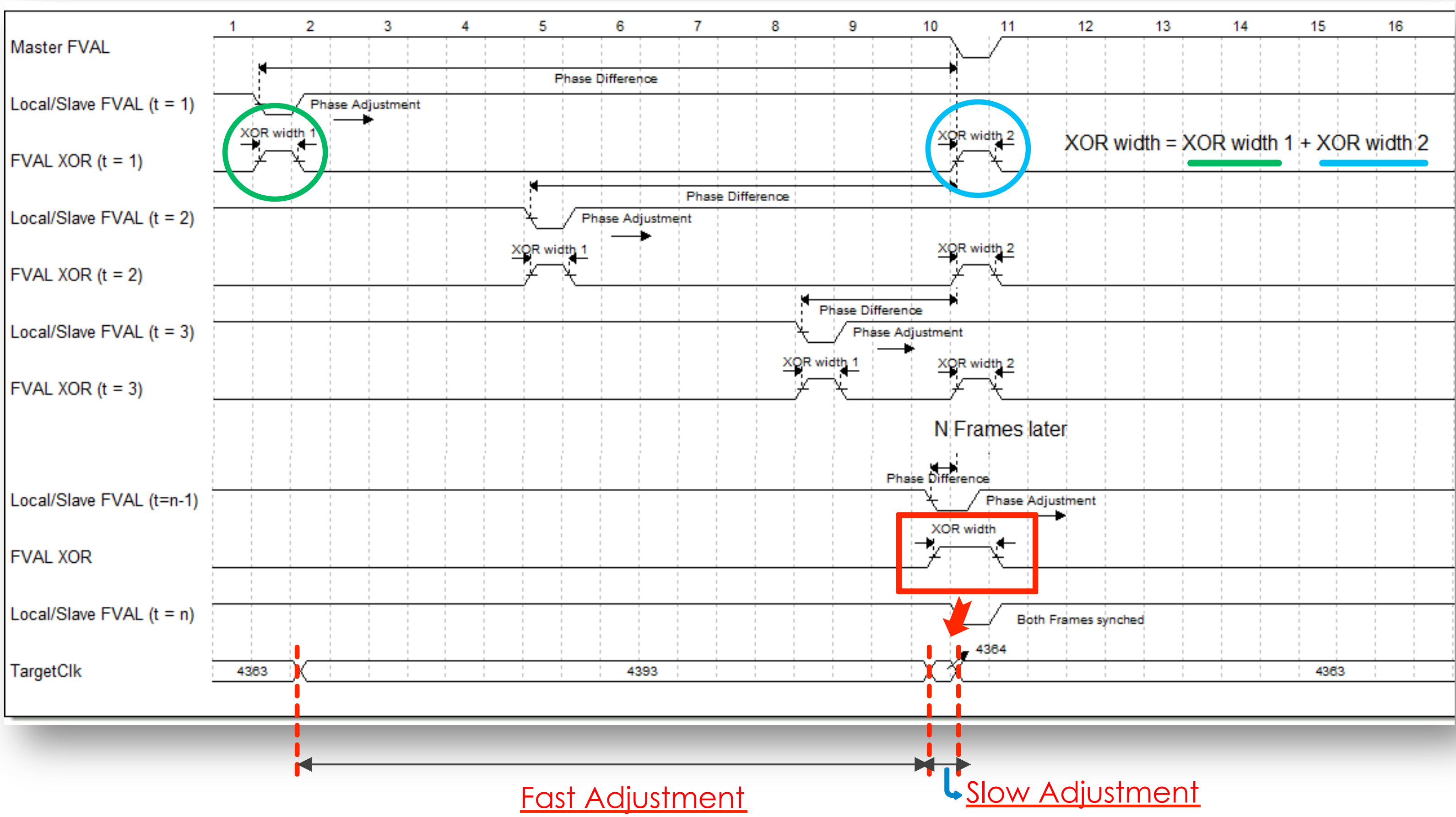
Phase-Frequency Synchronization Achieved!!

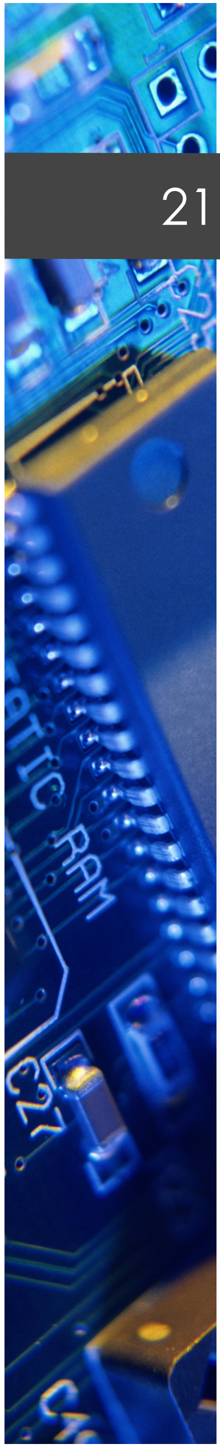
However, the adjustment speed is <u>LOW</u>

Multi-Camera Synchronization Core

Proposed Solution

Phase Correction (Fast Adjustment)

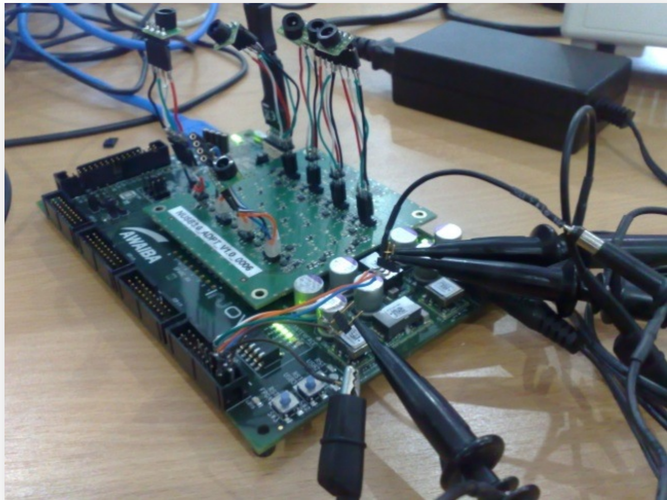


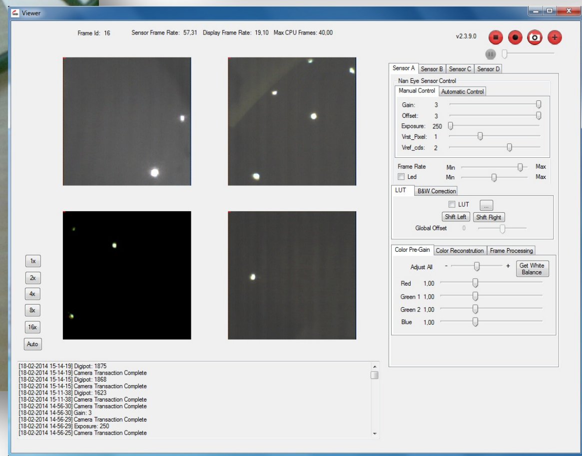


Multi-Camera Synchronization Core

Results

- **System Composition**
  - Up to 4 NanEye
  - NanoUSB2 and DisposcopeUSB3 platforms
  - Digital scope
  - Video data reception and register command sending through USB2/3
  - Awaiba Viewer



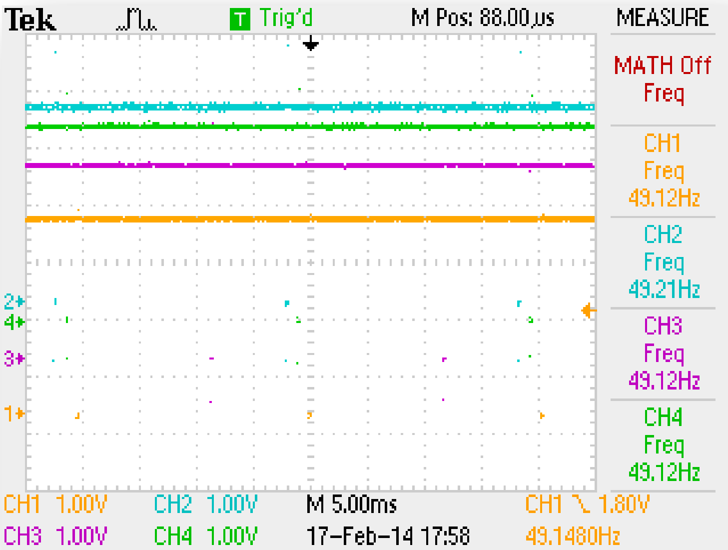


FPGA: Spartan 3E
Spartan 6

Multi-Camera Synchronization Core

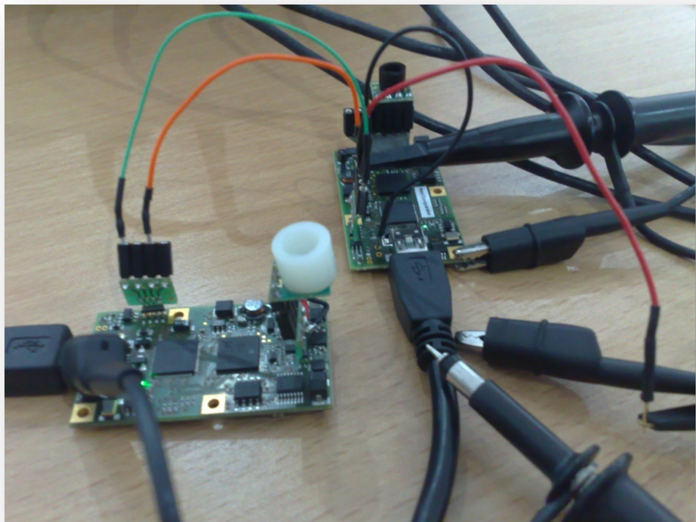
Results

Synchronism between 2 Sensors



Phase offset between frames of different cameras

Use of the MASTER-SLAVE control scheme

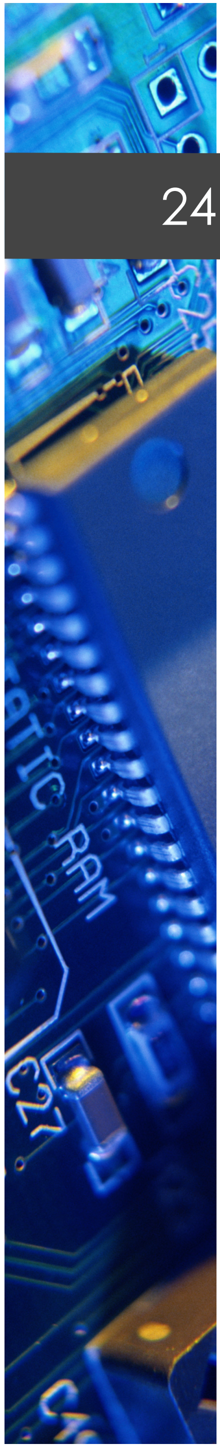


Exchange of control signals between the GPIO connectors of two NanoUSB2 boards

Multi-Camera Synchronization Core

Results

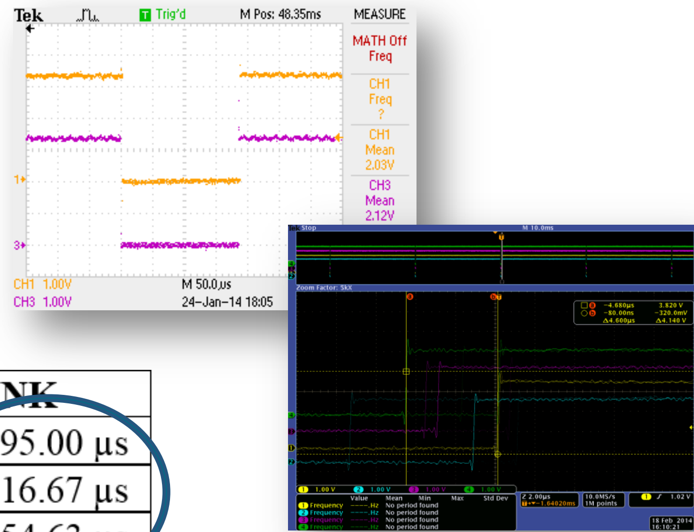
- **Synchronism between 2 Sensors**



Multi-Camera Synchronization Core

Results

Phase Error



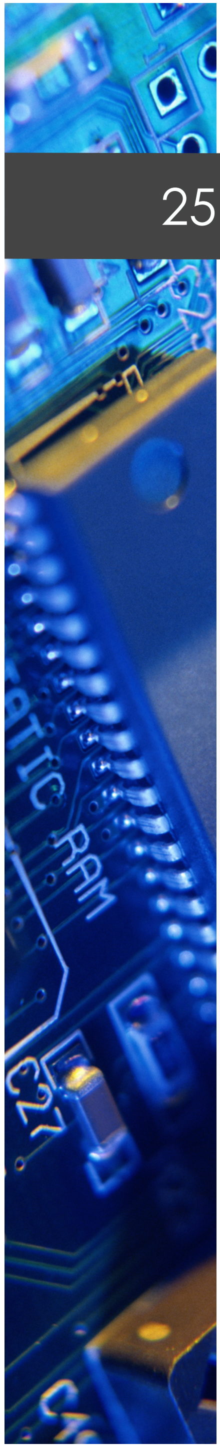
NanoUSB2 Platform		MATLAB/SIMULINK	
$Max(\varphi_{Error})_{NanoUSB2}$	5.80 µs	$Max(\varphi_{Error})_{Simulink}$	95.00 µs
$Min(\varphi_{Error})_{NanoUSB2}$	0.40 µs	$Min(\varphi_{Error})_{Simulink}$	16.67 µs
$Avg(\varphi_{Error})_{NanoUSB2}$	3.82 µs	$Avg(\varphi_{Error})_{Simulink}$	54.63 µs

Model used on the simulation was overly pessimistic

NanoUSB2 Platform		DisposcopeUSB3 Platform	
$Max(\varphi_{Error})_{NanoUSB2}$	5.80 µs	$Max(\varphi_{Error})_{DisposcopeUSB3}$	8.76 µs
$Min(\varphi_{Error})_{NanoUSB2}$	0.40 µs	$Min(\varphi_{Error})_{DisposcopeUSB3}$	0.58 µs
$Avg(\varphi_{Error})_{NanoUSB2}$	3.82 µs	$Avg(\varphi_{Error})_{DisposcopeUSB3}$	3.77 µs

The error on both platforms is very similar

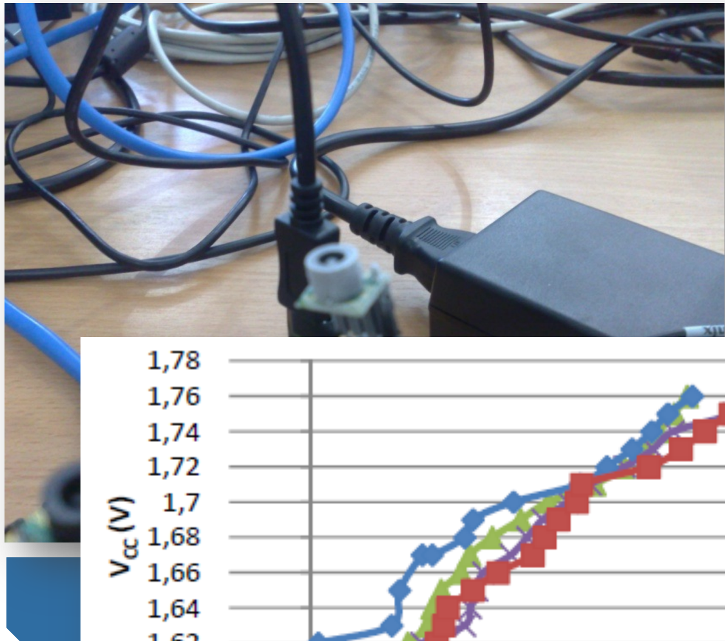
Considering that the nominal Frame Rate of a NanEye camera is 44 fps, this means that the average phase error is ~0,017%!!

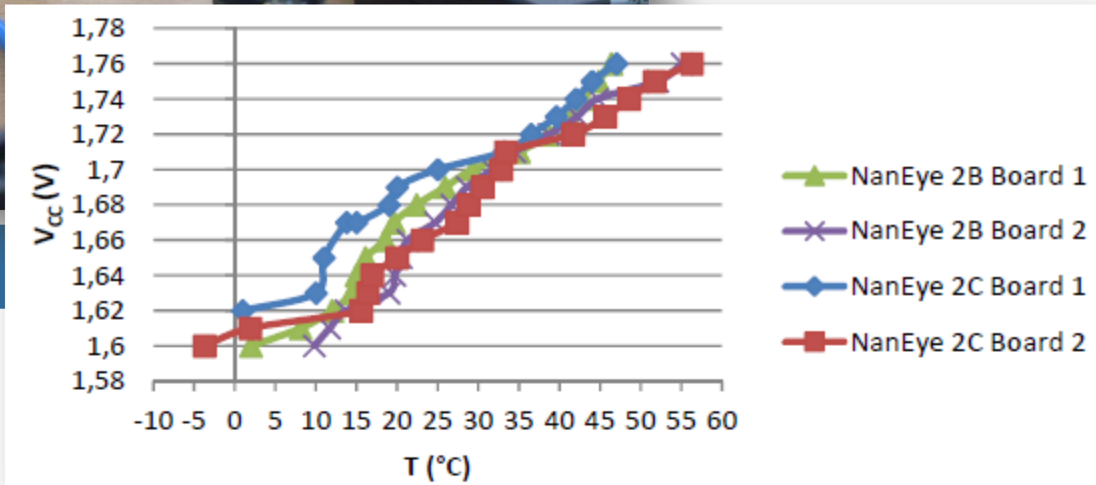


Multi-Camera Synchronization Core

Results

- **Temperature Dependency**

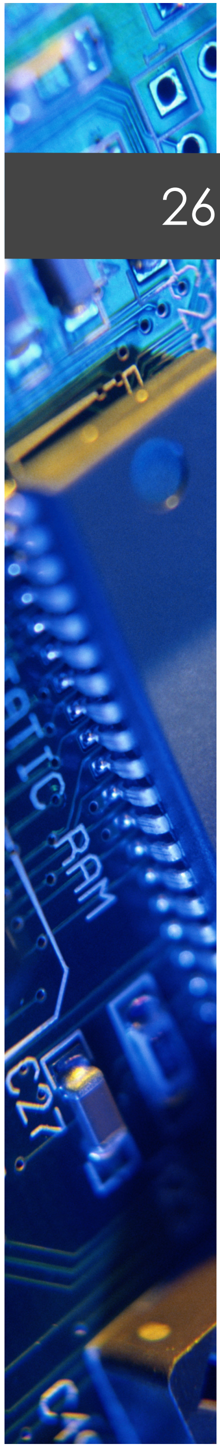




Power supply variation as a function of temperature

- The frequency of an Oscillator Ring has a great dependency on temperature
- Hence the frame rate on each camera was fixed to the same value
- And the system submitted to temperature differences of 50 °C between sensors
- Up to 4 Sensors were tested simultaneously

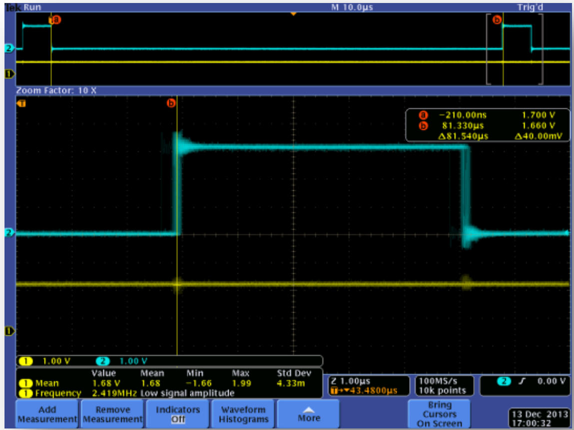
Vc applied on each sensor must be individually and dynamically modulated to compensate the temperature differences between sensors in order to maintain phase-frequency synchronism!



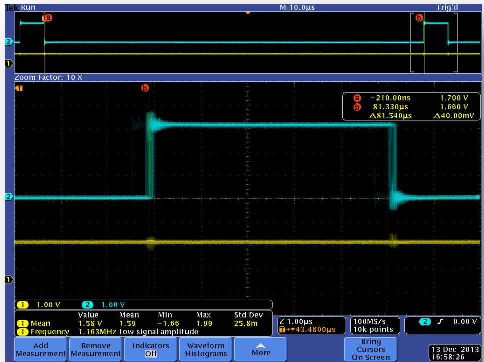
Multi-Camera Synchronization Core

Results

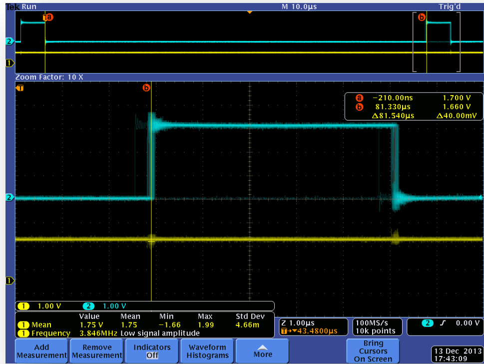
- **Temperature Dependency (1 sensor)**



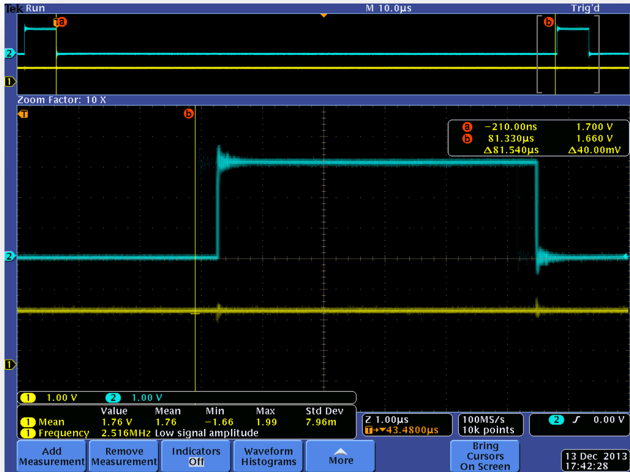
Vc = 1.68 V - T = 22.4 °C



Vc = 1.58 V - T = 2 °C

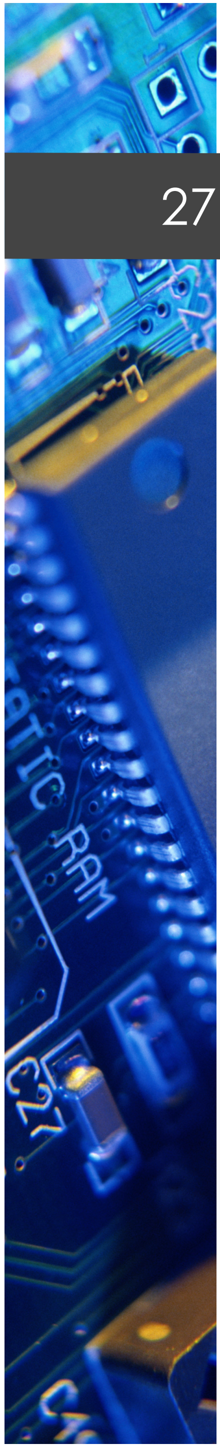


Vc = 1.75 V - T = 44.8 °C



Vc = 1.76 V - T = 46.4 °C

The Line Rate is stable as long as T is kept within the dynamic range of Vc

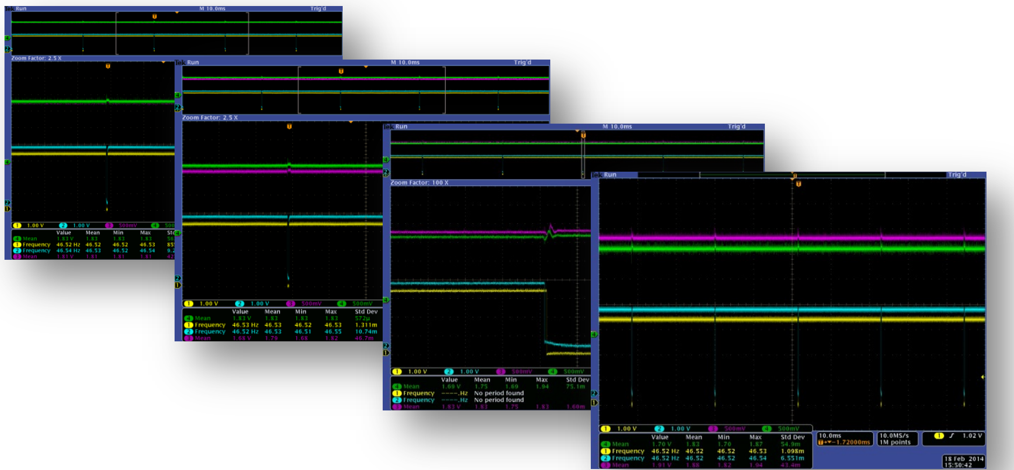


Multi-Camera Synchronization Core

Results

- **Temperature Dependency (2 sensors)**

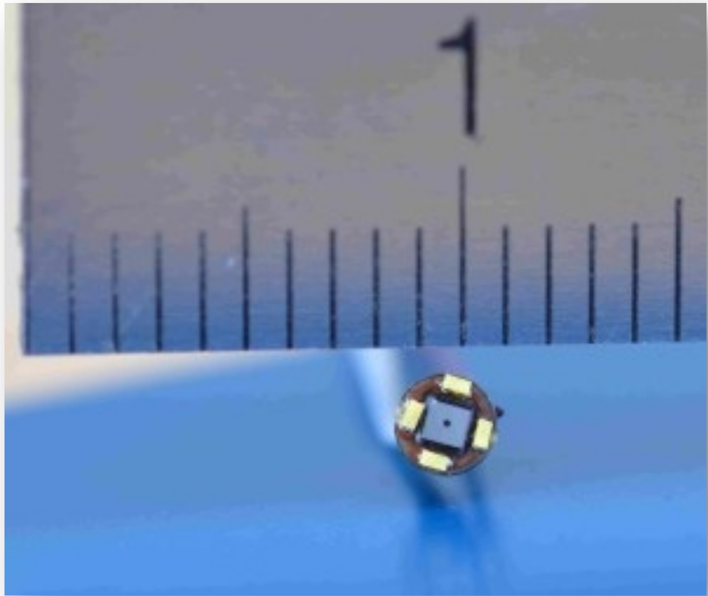
Sensor A			Sensor B			
Temperature (°C)	V_{CC} Voltage (V)	Frame Rate (fps)	Temperature (°C)	V_{CC} Voltage (V)	Frame Rate (fps)	Instantaneous φ_{Error} (µs)
22.9	1.81	46.54	22.9	1.83	46.52	25
-1.2	1.68	46.52	23.1	1.83	46.53	7
22.5	1.83	46.52	-1.7	1.69	46.52	8
59.7	1.91	46.52	0.9	1.70	46.52	4



The Phase-Frequency Synchronism is maintained even in the presence of a ΔT of 58,8 °C!

Advanced illumination control algorithm in VHDL

Motivation



<u>Need for illumination in several medical procedures</u>

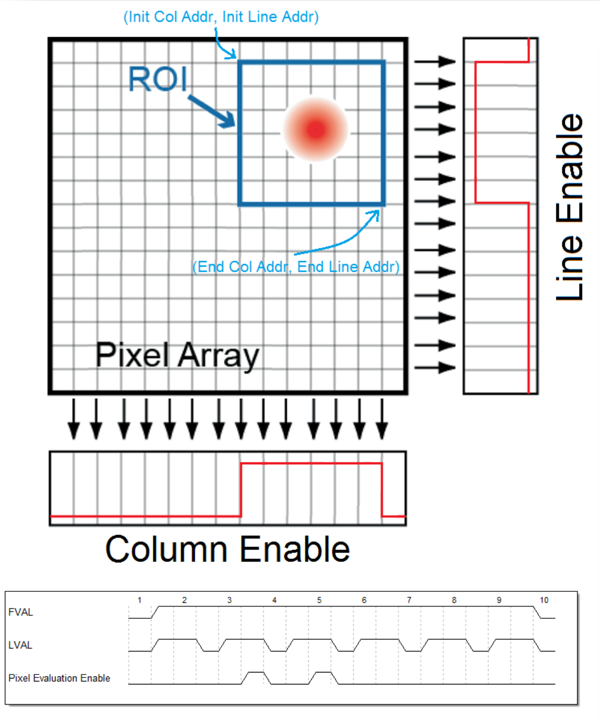
Automatic adaptation of light intensity, according to the illumination level

- Caracteristics:
  - **Can work with the sincronization system**
  - Compact System:
    - **LED ring**
    - **Fiber light source**
  - **Uses NanoUSB2 platform**

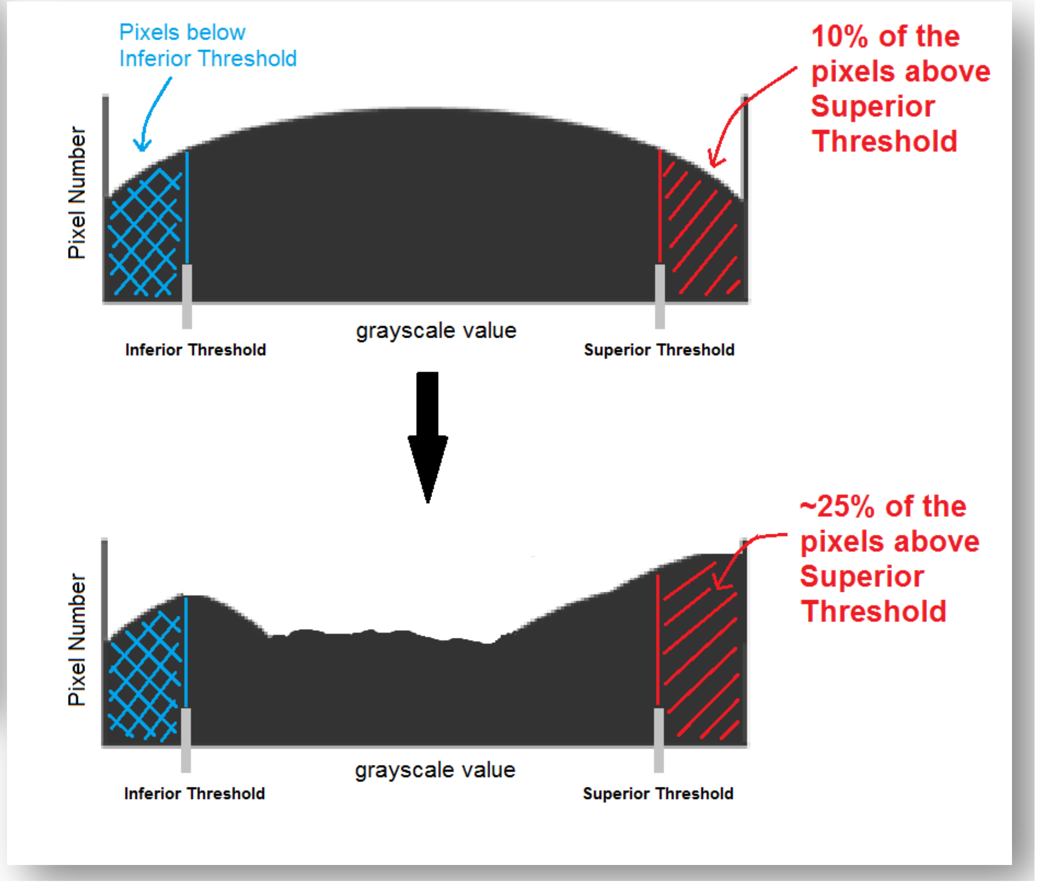
Advanced illumination control algorithm in VHDL

Proposed Solution

- **Definition of a ROI**

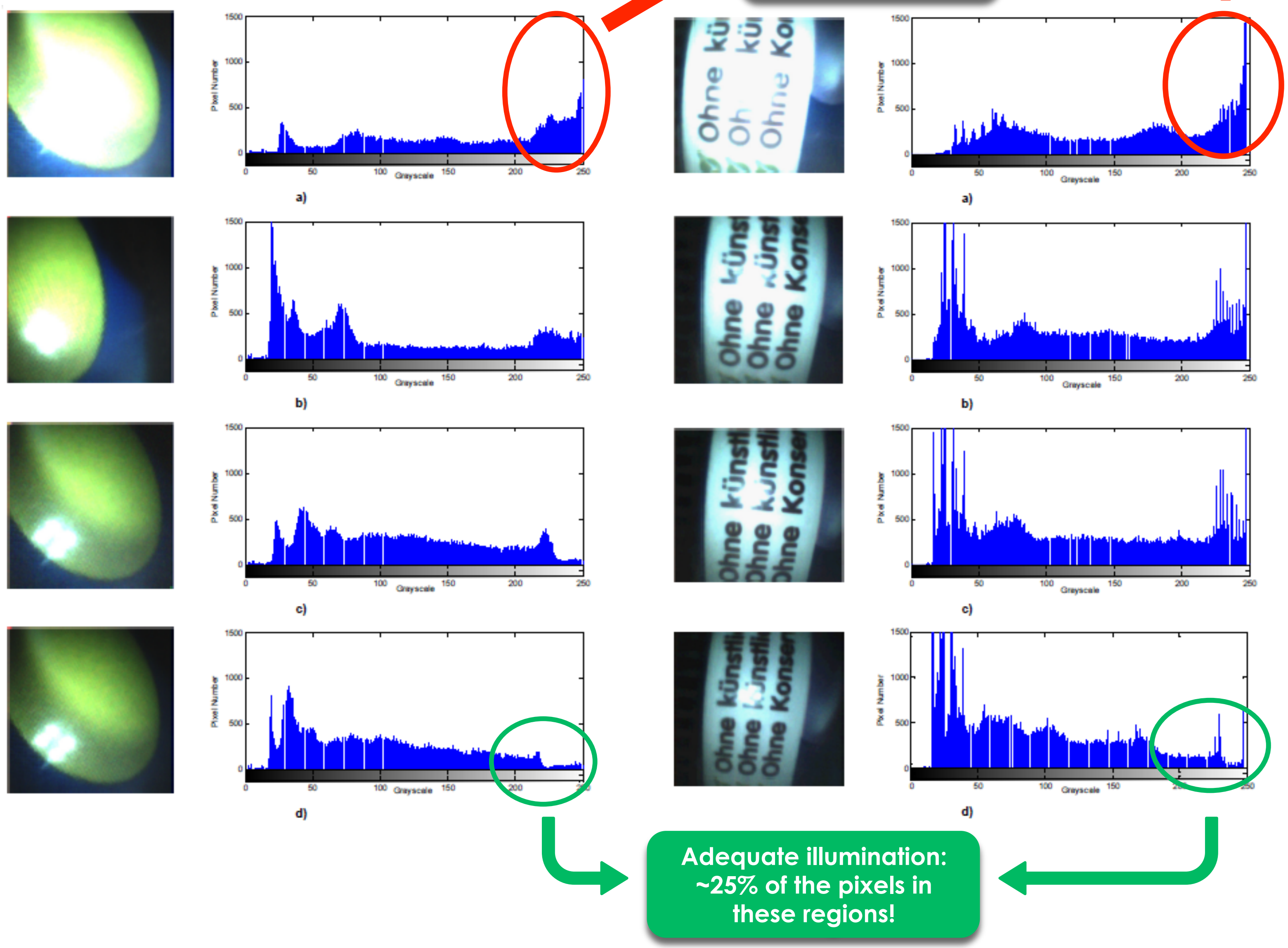


- **Control Algorithm based on Histogram information**



Results

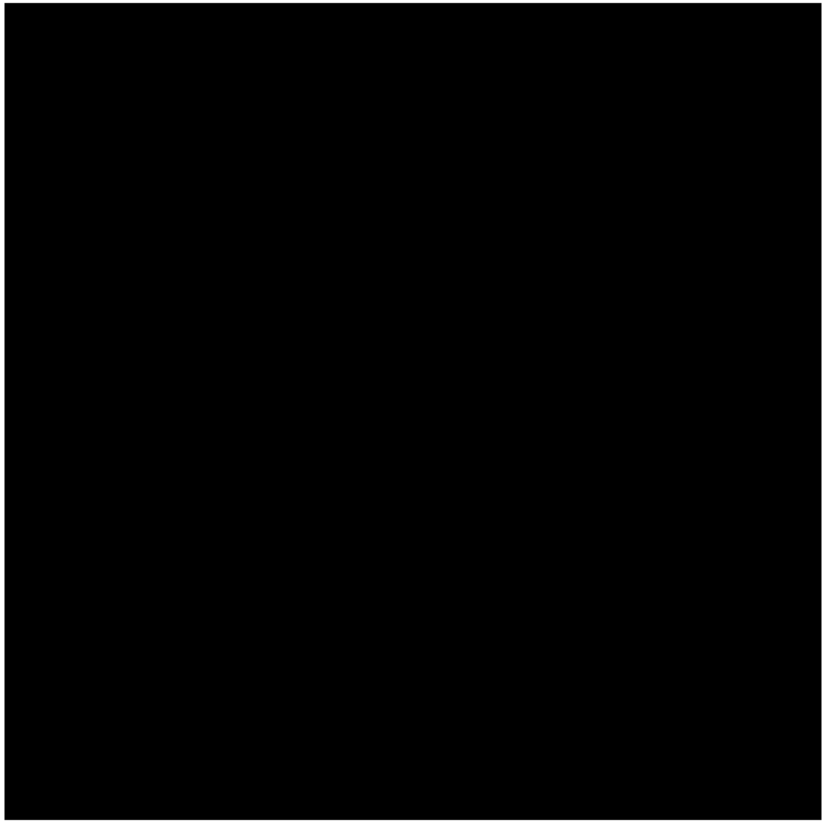
- Illumination level adjustment

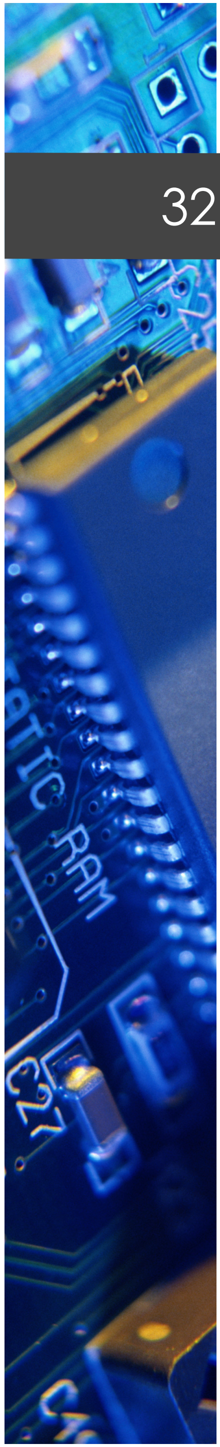


Advanced illumination control algorithm in VHDL

Results

- **Illumination level adjustment**





Advanced illumination control algorithm in VHDL

Results

- **Illumination level adjustment**

Development	1st stage	2nd stage	3rd stage	4th stage	5th stage
Error	< 1%	< 12%	< 12%	< 3%	<3%
Adjustment speed	> 10 s	2,5 s a 3,5 s	2 s a 3 s	4 s a 5 s	0,5 s a 1 s
Stability	+++	--	-	++	+
Used hardware	--	-	+	++	+++

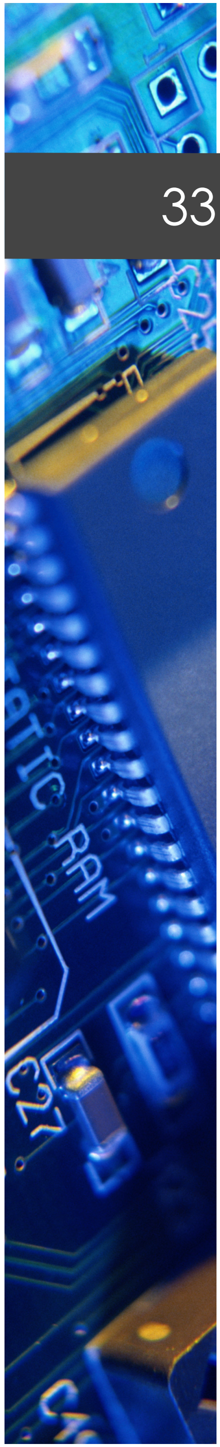
1st stage: Unitary step adjustment

2nd stage: Error based Multi-level step adjustment

3rd stage: Flags for last correction direction

4th stage: Integrative component added

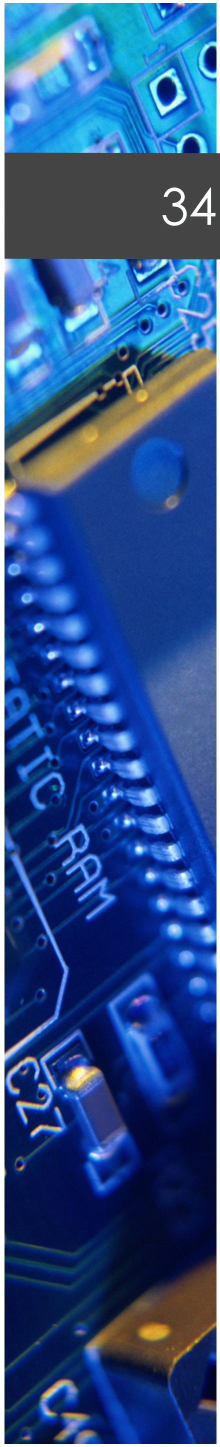
5th stage: Derivative component added



Conclusion

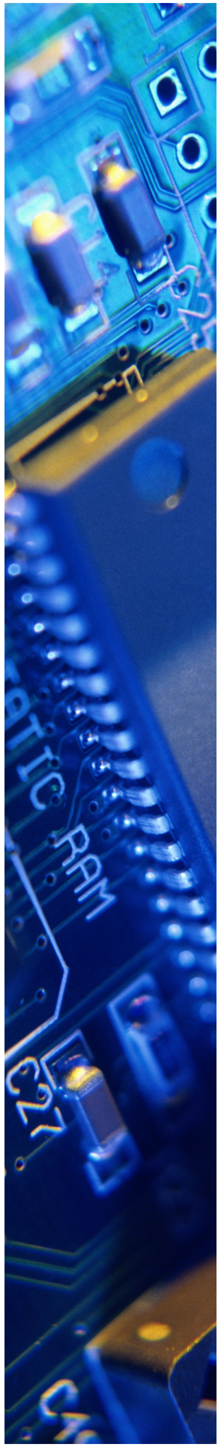
- The frequency control method presented here is characterized by its:
  - Simplicity
  - Portability
  - Replicability

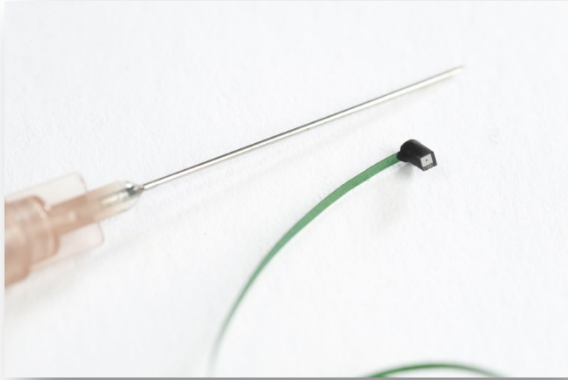
- The multi-camera phase-frequency synchronization was achieved regardless of:
  - **Ambient temperature**
  - **Sensor version**
  - **FPGA platform**
  - **Cable length**



Conclusion

- However the control system is limited by the operational range of the camera itself (power supply range).
  - On the other hand, it proved capable of regaining synchronization after large offsets had occurred.
- The illumination control algorithm has shown to be capable of maintaining an adequate light level, based on the image histogram.
  - It allows optimizing illumination in configurable regions of interest
  - The algorithm was implemented minimizing the amount of resources used





Thank You!!

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